LOW POWER FLASH MEMORY CELL AND METHOD

CROSS-REFERENCE

This application is a continuation-in-part of U.S. Patent Application No. 10/112,014, filed on March 29, 2002, entitled Method of Making Self-Aligned Shallow Trench Isolation, which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

A flash memory cell may be formed on a substrate using a double polysilicon structure, with inter-poly oxide interposed between a floating polysilicon gate and a control polysilicon gate. A tunnel oxide is interposed between the floating polysilicon gate and the substrate.

The programming voltage of a flash memory cell is determined by the field required to generate tunnel current through the tunnel oxide, which is interposed between the floating polysilicon gate and the substrate, for example bulk silicon. The thinner the tunnel oxide and the inter-poly oxide the lower the programming voltage will be. As the oxide layers are thinned, the leakage current increases and the charge retention time is reduced. The required charge retention time sets the lower limit of the thickness of both the tunnel oxide and the inter-poly oxide.